AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 12, line 10, with the following rewritten paragraph:

Once the SRAM cache 34 mounted on the ceramic substrate 32 is tested and deemed satisfactory, the ~~combined cache 34 and~~ side of the substrate 32 that does not have the SRAM 34 cache mounted to it ~~substrate 32~~ is attached to a shelf 18 of ceramic package 17, with the ceramic substrate 32 functioning as a lid above the CPU die 26 (step 62). Note that substrate 32 can have a metallized surface for traces, or can utilize a multi-layer ceramic approach. Regardless, the substrate 32 can function both as a lid for the multi-chip package 10 as well as a component for carrying a device such as the SRAM cache 34. A seal 42 is between the base of the substrate 32 and the upper edge of the shelf 18 it resides on. In one embodiment, the seal 42 is an eutetic seal; the seal 42 may also be an epoxy. In this manner, an open cavity 44 with no filler protects the CPU die 26. The seal 42 provides an environmental seal in addition to providing structural support between substrate 32 and package 17.--

Please replace the paragraph beginning at page 14, line 1, with the following rewritten paragraph:

--Once the SRAM cache 74 mounted on the ceramic substrate 32 is tested and deemed satisfactory, the ~~combined cache 74 and substrate 32~~ side of the substrate 32 that does not have the SRAM cache 74 mounted to it is attached to a shelf 18 of ceramic package 17, with the ceramic substrate 32 functioning as a lid above the CPU die 26 (step 62). A seal 42 is between the base of the substrate 32 and the upper edge of the shelf 18 it resides on. In this manner, an open cavity 44, with no filler

protects the CPU die 26. After the substrate 32 has been attached and sealed to the shelf 18 of the ceramic package 17, the substrate 32 is electrically connected to the ceramic pakage 17 using wire bond II 38 (step 64). In this manner, the SRAM cache 74 is electrically coupled to the chip package 17. The multi-chip package 70 is then filled (above the SRAM cache 34 and substrate 32) with an encapsulant 40 (step 66). Once the multi-chip package 70 is fully fabricated, a final functionality test may be applied to the device as a whole (step 68).--

Please replace the paragraph beginning at page 15, line 14, with the following rewritten paragraph:

--Once the SRAM cache 74 mounted on the organic substrate 91 is tested and deemed satisfactory, the ~~combined cache 74 and substrate 91~~ side of the substrate 91 that does not have the SRAM cache 74 mounted to it is attached to a shelf 18 of organic package 93, with the organic substrate 91 functioning as a lid above the CPU die 26 (step 110). A seal 42 is between the base of the substrate 91 and the upper edge of the shelf 18 it resides on. After the substrate 91 has been attached and sealed to the shelf 18 of the organic packago the organic package 93 using wire bonds II 38 (112). In this manner, the SRAM cache 74 is electrically coupled to the chip package 93. The multi-chip package 90 is filled (above the SRAM cache 74 and substrate 91) with a second encapsulant 40 (step 114). Once the multi-chip package 90 is fully fabricated, a final functionality test may be applied to the device as a whole (step 116).--

Please replace the paragraph beginning at page 16, line 20, with the following rewritten paragraph:

Once the SRAM cache 132 mounted on the ceramic substrate 128 is tested and deemed satisfactory, the ~~combined cache 132 and substrate 128~~ side of the substrate 128 that does not have the SRAM cache 132 mounted to it is attached to a shelf 16 of organic package 93, with the ceramic substrate 128 functioning as a lid above the semiconductor die 124. After the substrate 128 has been attached and sealed to the shelf 16 of the organic package 93, the substrate 128 is electrically connected to the organic package 93 using wire bond III 136. In this manner, the SRAM cache 132 is electrically coupled to the chip package 93. The multi-chip package 118 is filled (above the SRAM cache 132 and substrate 128) with an encapsulant 138. The partially fabricated multi-chip package 118 may be tested for functionality at this stage of fabrication also before proceeding.

LISTING OF THE CLAIMS:

28. (currently amended) A method of constructing a multi-chip package, comprising:

electrically connecting a semiconductor die to at least one of a plurality of shelves;

electrically connecting a flip-chip to a ~~ceramic~~ substrate; and

attaching ~~said ceramic substrate~~ the side of said substrate that does not have the flip-chip mounted to it to one of said plurality of shelves.

29. (currently amended) The method of claim 28, further comprising electrically connecting said ~~ceramic~~ substrate to at least one of said plurality of shelves.

30. (currently amended) The method of claim 29, wherein electrically connecting said ~~ceramic~~ substrate to at least one of said plurality of shelves comprises electrically connecting said ~~ceramic~~ substrate to at least one of said plurality of shelves with at least one bond wire.

31. (currently amended) The method of claim 28, wherein attaching the side of said ~~ceramic~~ substrate that does not have the flip-chip mounted to it to one of said plurality of shelves provides a lid above said semiconductor die.

32. (currently amended) The method of claim 28, further comprising electrically testing said electrically connected flip-chip before attaching of said ~~ceramic~~ substrate to said one of said plurality of shelves.

33. (currently amended) The method of claim 28, wherein electrically connecting said flip-chip to said ~~ceramic~~ substrate comprises electrically connecting said flip-chip to said ~~ceramic~~ substrate with solder balls.

34. (previously added) The method of claim 28, further comprising covering said flip-chip with an encapsulant.

35. (currently amended) The method of claim 28, further comprising disposing a seal between a base of said ~~ceramic~~ substrate and one of said plurality of shelves to which said ~~ceramic~~ substrate is attached.

36. (previously added) The method of claim 28, wherein electrically connecting said semiconductor die to said at least one of a plurality of shelves comprises electrically connecting a CPU chip to said at least one of said plurality of shelves.

37. (currently amended) The method of claim 28, wherein electrically connecting said flip-chip to said ~~ceramic~~ substrate comprises electrically connecting a memory cache

flip-chip to said ~~ceramic~~ substrate.

38. (previously added) The method of claim 28, wherein electrically connecting said semiconductor die to at least one of said plurality of shelves comprises electrically connecting said semiconductor die to said at least one of a plurality of shelves with at least one bond wire.

39. (previously added) The method of claim 28, further including attaching said semiconductor die to a slug.

40. (previously added) The method of claim 39, further comprising attaching said slug to at least one of a plurality of shelves.

REMARKS

In the specification, the paragraphs beginning at page 12, line 10, page 14, line 1, page 15, line 14, and page 16, line 20, have been amended to describe mounting the side of the substrate that does not have the SRAM 34 cache mounted to it to a shelf of the package, as originally disclosed in FIGS.1, 3, 5 and 7.

Claims 28-40 remain in the application. Independent claim 28 has been amended to include the limitations of attaching the side of the substrate that does not have the flip-chip mounted to it to one of said plurality of shelves, as disclosed in the amended specification as described above. Dependent claims 29-33 and 35, 37 have been amended to reflect this change. No new subject matter has been added with these amendments.

A. Comment

The examiner pointed out that the Applicant cancelled the wrong set of claims. The Applicants agree that the correct set of claims that should have been cancelled was 21-27.

B. 35 U.S.C. § 102

Claims 28, 29, 31-33 and 35-40 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,874,321 issued February 23, 1999 to Thomas Templeton, et al. (hereinafter "the Templeton patent") (Office Action, page 3).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Regarding claim 28, independent claim 28 has been amended to include the limitations of attaching the side of the ceramic substrate that does not have the flip-chip mounted to it to one of said plurality of shelves. The Templeton patent discloses attaching the side of the ceramic substrate that has the flip-chip mounted to it to one of said plurality of shelves, not the side that doesn't have the flip-chip mounted to it. The Templeton patent does not disclose each and every element of claim 28, thus, claim 28 is not anticipated by the Templeton patent. Because claims 29, 31-33 and 35-40 depend from claim 28, claims 29, 31-33 and 35-40 are not anticipated by the Templeton patent. Therefore, reconsideration and withdrawal of the 102(e) rejection of claims 29, 31-33 and 35-40 is respectfully requested.

C. 35 U.S.C. § 103(a)

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Templeton in view of Gaudenzi - Claims 30 and 34

Claims 30 and 34 stand rejected under 35 U.S.C. § 103(a) as being obvious over the Templeton patent in view of the U.S. Patent No. 5,313,366 issued May 17, 1994 to Gene Gaudenzi, et al. (hereinafter "the Gaudenzi patent") (Office Action, page 4).

Regarding claim 30, the Office contends that while the Templeton patent does not disclose electrically connecting the substrate to at least one of the shelves with a wire bond, Gaudenzi discloses electrically connecting the substrate to at least one of the shelves with a wire bond. The Office maintains that it would have been obvious to incorporate wire bonding the substrate to a shelf with the invention of Templeton (Office Action, page 5).

Independent claim 28 (from which claim 30 depends) contains the limitations of attaching the side of the ceramic substrate that does not have the flip-chip mounted to it to one of said plurality of shelves of the multi-chip package. The Templeton patent discloses attaching the side of the ceramic substrate that has the flip-chip mounted to it to one of the plurality of shelves. Even though the it may have been obvious to incorporate wire bonding the substrate to a shelf with the invention of Templeton (the possibility of which the Applicants do not concede), neither the Tempelton patent nor the Gaudenzi patent disclose either alone or in combination attaching the side of the substrate that does not have the flip chip mounted to it to one of the shelves of a multi-chip package.

Regarding claim 34, the Office contends that the Gaudenzi patent discloses covering the flip chip with an encapsulant. (Office Action, page 5). While it may be true that the Gaudenzi patent discloses covering the flip chip with an encapsulant, neither the Tempelton patent nor the

Gaudenzi patent disclose either alone or in combination attaching the side of the substrate that does not have the flip chip mounted to it to one of the shelves of a multi-chip package.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In *re Royka*, 490 F.2d 981,180 USPQ 580 (CCPA 1974). Because the Templeton patent and the Gaudenzi patent, either alone or in combination, do not teach or suggest all of the claim limitations of claims 30 and 34, claims 30 and 34 are not rendered obvious by the Templeton patent in view of the Gaudenzi patent.

In view of the foregoing remarks, the Applicants request allowance of the application. Please forward further communications to the address of record. If the Examiner needs to contact the below-signed agent to further the prosecution of the application, the contact number is (503) 264-0944.

Respectfully submitted,

Dated: October 6, 2003

Kathy J. Ortiz
Agent for Applicants
Reg. No. 54,351

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

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